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10/725,513	12/03/2003	Farsheed Mahmoudi	15624-US	3777

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EXAMINER

CHAN, RICHARD

ART UNIT PAPER NUMBER

2618

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/08/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/725,513	<b>Applicant(s)</b> MAHMOUDI ET AL.	
	<b>Examiner</b> Richard Chan	<b>Art Unit</b> 2618	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a): In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11/16/2006.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 3-8, 12-15, and 17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |                                                                                      |                                                                   |
|--------------------------------------------------------------------------------------|-------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____                                                          | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 8 is rejected under 35 U.S.C. 102(e) as being anticipated by Manku (US 6,232,848).

With respect to claim 8, Manku discloses the high linearity, low power, low voltage active mixer for RF applications, comprising: an RF transconductance amplifier connected to the input of RF+ and RF- Fig.6, and to transform the input voltage  $V_{in}$  to current, the transconductance amplifier having a constant transconductance over a wide range of input differential voltages; a mixing stage 12 to down-convert the RF current to the desired IF; an ac-coupling stage between the RF transconductance amplifier and the mixing stage Fig.6 capacitors connected between amplifier and mixing stages; and an IF stage that converts an information bearing signal back to voltage IF+ and IF-, wherein the AC coupling between the RF transconductance amplifier and the mixing stage blocks the flicker noise associated with the RF transconductance amplifier, and hence reduces the total flicker noise output, which favors the design for direct conversion applications.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 3, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Manku (US 6,232,848) in view of Sorrels (US 6,813,485) and Watanabe (US 6,522,195 B2).

With respect to claim 3, Manku discloses the high linearity, low power, low voltage active mixer for RF applications, comprising: an RF transconductance amplifier connected to the input of RF+ and RF- Fig.6, and to transform the input voltage  $V_{in}$  to current, the transconductance amplifier having a constant transconductance over a wide range of input differential voltages; a mixing stage 12 to down-convert the RF current to the desired IF; an ac-coupling stage between the RF transconductance amplifier and the mixing stage Fig.6 capacitors connected between amplifier and mixing stages; and an IF stage that converts an information bearing signal back to voltage IF+ and IF-, and a p-channel single transistor transconductor and an n-channel single transistor transconductor, however does not specifically disclose wherein the transconductors with

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constant transconductance result in high linearity in terms of both IIP2 and IIP3 and wherein the RF transconductance amplifier comprises: a floating voltage source and a capacitive feed-forward path.

The Sorrels reference however discloses complimentary FET switch implementations of the invention (lower  $R_{ds,sub,on}$  -increased conversion efficiency, higher IIP2, IIP3, minimal current increase (+CMOS inverter), and lower re-radiation (charge cancellation) FIGS. 112 and 113. See 6.7.4 Paragraph [771]

It would have been obvious to one of ordinary skill in the art to implement the active mixer as disclosed by Manku with technique of achieving high linearity terms of the Intermodulation Interception points.

The Watanabe reference in Fig.2 however discloses an amplifier/transconductor circuit having a feed forward path comprising a capacitor 38 and a floating voltage  $V_{cc}$ .

It would have been obvious to one of ordinary skill in the art to implement a capacitive feed forward path as disclosed by Watanabe with the amplifier circuit as disclosed by Manku and Sorrels in order to obtain a cleaner signal between the two nodes.

With respect to claim 5, Manku, Sorrels, and Watanabe combined disclose a high linearity, low power, low voltage active mixer as in claim 3, Watanabe discloses wherein the floating voltage source in the RF transconductance amplifier allows the low voltage operation of the RF transconductor amplifier.

With respect to claim 6, Manku, Sorrels, and Watanabe combined disclose a high linearity, low power, low voltage active mixer as in claim 3, Manku continues to disclose wherein the RF transconductance amplifier is self-biased and does not require any additional biasing circuitry.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Manku (US 6,232,848) and Sorrels (US 6,813,485) and Watanabe (US 6,522,195 B2) in view of Werner (US 5,529,046).

With respect to claim 4, Manku, Sorrels, and Watanabe combined discloses the high linearity, low power, low voltage active mixer comprising a transconductor as in claim 3, however the none of the references specifically disclose wherein a body effect of the p-channel single transistor transconductor and of the n channel single transistor transconductor is eliminated to improve the linearity by obviating the threshold voltage modulation assisted nonlinearity.

The Werner reference however discloses wherein the body effect of the transistor should be cancelled thereby creating a system, which has higher linearity. (Col.8 lines 38-59)

It would have been obvious to one of ordinary skill in the art to implement the technique of canceling the body effect of a transistor as disclosed by Werner with the high linearity system of Manku, Sorrels, and Watanabe combined in order to achieve a higher linearity throughout the system by canceling out the body effect of a transistor.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Manku (US 6,232,848) and Sorrels (US 6,813,485) and Watanabe (US 6,522,195 B2) in view of Karanicolas (US 5,721,500).

With respect to claim 7, Manku, Sorrels, and Watanabe combined disclose a high linearity, low power, low voltage active mixer as in claim 3, however none of the references specifically disclose wherein the concept of current reuse has been introduced to decrease the power consumption of the design.

The Karanicolas reference discloses the concept of current reuse implemented on a circuit wherein the current flowing from a drain of the first device active is reused in the second active device.

It would have been obvious to one of ordinary skill in the art to implement the current reuse concept as disclosed by Karanicolas with the system disclosed by Manku, Sorrels, and Watanabe combined in order to save overall power for the system.

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (US 6,522,195) in view of Manku (US 6,232,848).

With respect to claim 12, Watanabe discloses an RF transconductance amplifier for use in a high linearity, low power, low voltage active mixer, the RF transconductance amplifier comprising a loading voltage source  $V_{cc}$ ; a capacitive feed-forward path 38;

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and a p-channel single transistor transconductor 66, however Watanabe does not specifically disclose the implementation of an n-channel single transistor transconductor.

The Manku reference however specifically discloses the use of a n-channel transistor within the amplifier used in a low voltage radio integrated circuit design.

It would have been obvious to one of ordinary skill in the art to implement an n-channel transistor within an amplifier as disclosed by Manku with the amplifier disclosed by Watanabe in order to output a current based on the differential voltage inputted into the system.

8. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (US 6,522,195) and Manku (US 6,232,848) in view of Werner (US 5,529,046).

With respect to claim 13, Watanabe and Manku combined disclose an RF transconductance amplifier as defined in claim 12, however neither references specifically disclose wherein a body effect of the p-channel single transistor transconductor and of the n-channel single transistor transconductor is eliminated to improve the linearity by obviating the threshold voltage modulation assisted nonlinearity.

The Werner reference however discloses wherein the body effect of the transistor should be cancelled thereby creating a system, which has higher linearity. (Col.8 lines 38-59)

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It would have been obvious to one of ordinary skill in the art to implement the technique of canceling the body effect of a transistor as disclosed by Werner with the high linearity system of Manku, Sorrels, and Watanabe combined in order to achieve a higher linearity throughout the system by canceling out the body effect of a transistor.

With respect to claim 14, Watanabe, Manku, and Werner combined disclose a high linearity, low power, low voltage active mixer as in claim 3, Manku continues to disclose wherein the RF transconductance amplifier is self-biased and does not require any additional biasing circuitry.

With respect to claim 15, Watanabe and Manku combined disclose the RF transconductance amplifier, as defined in claim 12, Watanabe continues to disclose wherein the floating voltage source  $V_{cc}$  causes the p-channel single transistor transconductor and Manku discloses wherein the n-channel single transistor transconductor to operate simultaneously in the active region over a wide range of input differential voltages thus resulting in improved linearity in terms of IIP2.

9. Claims 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Manku (US 6,232,848) in view of Sorrels (US 6,813,485) .

With respect to claim 17, discloses a high linearity, low power, low voltage active mixer for RF applications, comprising: and RF transconductance amplifier connected to

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the input of RF+ and RF- Fig.6 to transform the input voltage to current, the transconductance amplifier having a constant transconductance over a wide range of input differential voltages; a mixing stage 12 to down convert the RF current to the desired IF; an ac-coupling stage between the RF transconductance amplifier and the mixing stage Fig.6; and an IF stage that converts an information bearing signal back to voltage, however does not specifically disclose wherein excellent linearity (IIP2, IIP3) results and thereby renders the mixer suitable for a direct receiver.

The Sorrels reference however discloses complimentary FET switch implementations of the invention (lower  $R_{ds,sub,on}$  -increased conversion efficiency, higher IIP2, IIP3, minimal current increase (+CMOS inverter), and lower re-radiation (charge cancellation) FIGS. 112 and 113. See 6.7.4 Paragraph [771]

It would have been obvious to one of ordinary skill in the art to implement the active mixer as disclosed by Manku with technique of achieving high linearity terms of the Intermodulation Interception points.

### ***Response to Arguments***

10. Applicant's arguments filed 11/16/06 have been fully considered but they are not persuasive.

With respect to applicant's arguments regarding claim 3, applicant has disclosed that the Watanabe reference does not disclose the floating voltage source of the transconductance amplifier, however the examiner directs the applicant to Fig.2 at the Vbias input (Col.3 line 9-15) The Voltage Bias input for amplifier 60 forces the amplifier into normal operation.

With respect to applicant's arguments regarding to claim 3, applicant argues that the capacitor 38 of Fig.2 of Watanabe is a path to bypass the main the main circuit. However in claim 3, applicant discloses "a capacitive feed-forward path" the capacitor 38 can be read as a feed-forward path from input Sin through transistor 68 through capacitor 38. (Col.4 line 17-21)

With respect to applicant's arguments regarding to claim 3, applicant also argues that the transconductance amplifier has a constant transconductance over a wide range of input differential voltages. The examiner cites the Sorrels reference as meeting this limitation, in order for the reference to exhibit a high linearity in terms in Intermodulation Interception Points by creating minimal current increase (+CMOS inverter), and lower re-radiation (charge cancellation), thus having a constant transconductance over an increased dynamic range. (Col.86 line 36-43)

With respect to claim 5, applicant refers back to claim 3 wherein the Watanabe reference does not disclose the floating voltage source of the transconductance

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amplifier, however the examiner directs the applicant to Fig.2 at the Vbias input (Col.3 line 9-15) The Voltage Bias input for amplifier 60 forces the amplifier into normal operation.

With respect to applicant's arguments regarding claim 6, applicant argues the Manku reference does not mention that the amplifier is self biased, however the examiner directs the applicant to Col.2 line (50-34) wherein Vb (Bias Voltage) is aided by the cascade structure of the transistors. The case structure of the transistor require matching voltage to be applied to both the VB and the VIN, therefore based on the input voltage, the Bias voltage will be applied to the amplifier automatically.

With respect to applicant's arguments regarding claim 4, the applicant admits that the Werner reference does teach the body-effect elimination to improve linearity, however the applicant discloses that the Werner reference is referred to high voltage power MOS devices. The examiner has taken such a limitation into consideration, however the structure of the claim's limitation still reads on the Werner reference. Details of the CMOS device as described by the applicant in the argument section are not within the claim language, therefore will not be give any patentable weight.

With respect to applicant's arguments regarding claim 7, please refer back to arguments regarding claim 3.

With respect to claim applicant's arguments regarding claim 8, applicant states that the Manku reference discusses the use of the capacitive coupling in order to achieve low-voltage operation, however does not discuss the capacitive coupling to filter out flicker noise. However the examiner directs the applicant to Col.4 line 63-Col.5 line 3, where Manku discloses the capacitive coupled resonating circuit to satisfy the filtering requirements imposed on the circuit.

With respect to applicant's arguments regarding claim 12, the applicant argues that the P-Channel FET disclosed by Manku is not a transconductor, while in fact is a bypass. The examiner believes that the P-Channel FET still acts as a transconductor for the BYPASS signal.

The applicant continues to argue the capacitor element 38 as having nothing to do with the feed-forward capacitor, the examiner respectfully disagrees and refer the applicant to arguments with claim 3.

The applicant continues to argue to that the floating voltage sources of the Watanabe reference, however the examiner directs the applicant to the Vbias input port on Fig.2 which is being labeled as the floating point voltage source.

With respect to applicant's arguments regarding claim 13, the applicant discloses that the Werner reference does not disclose the body-effect elimination to improve

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linearity. The applicant admits that the Werner reference does teach the body-effect elimination to improve linearity, however the applicant discloses that the Werner reference is referred to high voltage power MOS devices. The examiner has taken such a limitation into consideration. Please refer to remarks regarding claim 4.

With respect to applicant's arguments regarding to claim 14, please refer to remarks for claim 6.

With respect to applicant's arguments regarding to claim 15, the examiner refers to remarks for claim 12.

### ***Conclusion***

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Chan whose telephone number is (571) 272-0570. The examiner can normally be reached on Mon - Fri (9AM - 5PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on (571)272-7882. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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2/1/07



  
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